SC11876TP D01 AJ

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
12 July 2001 (12.07.2001)

PCT

(10) International Publication Number
WO 01/50504 A2

(51) International Patent Classification[7]: H01L 21/00

(21) International Application Number: PCT/US00/35130

(22) International Filing Date:
22 December 2000 (22.12.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/475,333 30 December 1999 (30.12.1999) US

(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(71) Applicant *(for MC only)*: PHILIPS SEMICONDUCTORS, INC. [US/US]; 1000 West Maude Avenue, Sunnyvale, CA 94085 (US).

(72) Inventors: HALEY, Mark, W.; 2750 CR 2615, Rio Medina, TX 78066 (US). PARKS, Delbert; 7911 Beechnut Park, San Antonio, TX 78240 (US).

(74) Agent: CRAWFORD, Robert, J.; Crawford PLLC, Suite 390, 1270 Northland Drive, Saint Paul, MN 55120 (US).

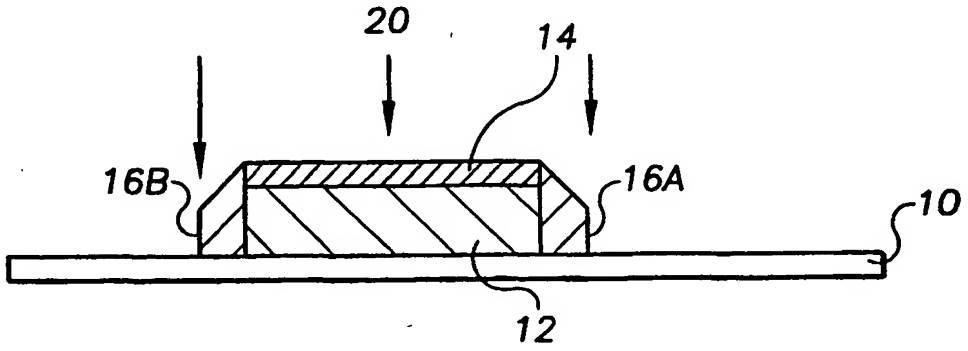
(81) Designated States *(national)*: CN, JP, KR.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *Without international search report and to be republished upon receipt of that report.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: AN IMPROVED METHOD FOR BURIED ANTI-REFLECTIVE COATING REMOVAL



(57) Abstract: A method for manufacturing a semiconductor structure, having a substrate and a gate region thereon, is described that includes removing an anti-reflective coating (ARC) layer over the gate region to improve salicidation of the gate. An anti-reflective coating is formed over the gate region and then a dielectric layer is formed over the anti-reflective coating layer and the substrate. Dielectric spacers are then formed on the substrate, adjacent the gate region and the anti-reflective coating layer, by etching the dielectric layer using a first process that includes selectively removing portions of the dielectric layer on the anti-reflective coating. Utilizing a second, different etching process, the anti-reflective coating over the gate region is selectively removed while preserving the spacers adjacent the gate region. Use of the present invention helps to minimize the dielectric spacer loss along side the gate region during removal of the buried anti-reflective coating, thereby providing a protection to the gate edge during the salicidation.

WO 01/50504 A2

AN IMPROVED METHOD FOR BURIED ANTI-REFLECTIVE COATING REMOVAL

Field of the Invention

The present invention is generally directed to semiconductor structures using anti-reflective coatings to aid in the photolithography process as well as semiconductor structures utilizing spacers adjacent the gate regions for forming source and drain regions.

Background of the Invention

Tremendous advances in semiconductor technology have permitted dramatic increases in circuit density and complexity with equally dramatic decreases in power consumption and package sizes. Single-chip microprocessors with millions of transistors, operating at speeds of hundreds of MIPS (millions of instructions per second), are packaged in relatively small, air-cooled semiconductor device packages. Many of the integrated circuits formed on semiconductor substrates are comprised of several circuit functions now all integrated on the single chip. For example, nonvolatile memory (NVM) devices, such as DRAMs (dynamic random access memory), are composed of an array of memory cells for storing digital information. The peripheral circuits on these devices are typically composed of logic circuits for addressing the memory cells, while other peripheral circuits function as read/write buffers and sense amplifiers. Commercially, the drive for increased portability and continuous use, while reducing size and weight, of electronic hand held devices has put more pressure on chip manufacturers to find ways to handle these requirements while reducing the chip size.

The combination of decreasing geometries in chips and the increase in the use of highly reflective materials, such as polysilicon, aluminum and metal silicides has lead to increased photolithographic patterning problems. Unwanted reflections from these underlying reflective materials during the photoresist patterning process often cause the resulting photoresist patterns to be distorted. Further, in order to fabricate high

performance MOS transistors it is necessary to control gate electrode linewidths. Improved control of the gate electrode linewidth allows the formation of smaller channel lengths and increases the performance of MOS transistors. Poor photoresist patterning can lead to varying linewidths and to varying gate-lengths, which ultimately lead to variations in the channel length. Consequently, variation of the channel length will alter the electrical characteristics of the MOS device which are supposed to be carefully controlled.

One current technique for improving gate electrode linewidth control in manufacture of MOS transistors involves the use of amorphous silicon deposition. Amorphous silicon deposition eliminates the replication of underlying isolation topography in the polysilicon surface. However, amorphous silicon deposition has problems with deposition defects and is also more difficult to fully dope.

Another technique for improving linewidth control involves the use of anti-reflective layers as part of the photolithographic process. The use of anti-reflective layers reduces the effects of both the surface roughness caused by the grain structure of polysilicon and the resist thickness variation due to the underlying effects caused by the rough surface and the topographical features of the polysilicon layer. The addition of an anti-reflective layer also helps to planarize the isolation topography and reduce the variation of the photoresist thickness over the substrate. The benefits of using anti-reflective coatings (ARC) can be lost if the coatings can not be totally and easily removed prior to silicide formation (contact formation), since the use of ARCs already require special processing equipment and can add additional steps a manufacturing process.

Where a buried anti-reflective coating (BARC) on a gate region is used in manufacturing a semiconductor device, it is necessary to remove all of the BARC prior to proper salicidation of the gate. Incomplete BARC removal causes poor silicide formation on the top of the gate. Oxide spacers may also be included as part of the device's structure, the formation of which tend to complicate the BARC removal process. Removal of the BARC film during spacer etching has led to narrow spacer

profiles and excessive isolation oxide loss. Overetching of the oxide spacer layer has been attempted to solve the problem of incomplete BARC removal, but this has led to degradation of the device's structure and performance.

Therefore, there is a need to provide a method for effectively and selectively removing the entire anti-reflective coating on a device prior to silicide formation without substantially disrupting the adjacent insulative structures or the underlying amorphous silicon layer. Further, there is a need for a method of removing the ARC layer that can be easily integrated into the process flow of conventional manufacturing techniques for semiconductor devices.

Summary of the Invention

In the present invention a two step etching process is used to remove substantially all of an anti-reflective coating from a gate region while minimizing the dielectric spacer loss along side the gate. Minimizing spacer oxide loss along side the gate, in turn, provides protection to the gate edge during the silicidation which prevents notching at the top of the gate.

An example embodiment of the present invention is directed to a method for manufacturing a semiconductor structure, having a substrate and a gate region thereon, which includes removing an anti-reflective coating (ARC) layer over the gate region to improve silicidation of the gate. An anti-reflective coating is first formed over the gate region. A dielectric layer is formed over the anti-reflective coating layer, the gate region and the substrate. Dielectric spacers are then formed on the substrate, adjacent the gate region and the anti-reflective coating layer, by etching the dielectric layer using a first process that includes selectively removing portions of the dielectric layer on the anti-reflective coating. Utilizing a second, different etching process, the anti-reflective coating over the gate region is selectively removed while preserving the spacers adjacent the gate region.

Another example embodiment of the present invention is directed to a method for manufacturing a semiconductor structure, having a substrate and a gate region

thereon, which includes the removal of an anti-reflective coating (ARC) layer over the gate region to improve silicidation of the gate. The method includes providing an buried anti-reflective coating over the gate region and providing an oxide layer over the buried anti-reflective coating layer, the gate region and the substrate. Oxide spacers are formed on the substrate, adjacent the gate region and the anti-reflective coating layer, by using a first process to substantially simultaneously etch the oxide layer to form the spacers and to remove the oxide on the anti-reflective coating. Next, an endpoint is utilized to terminate the first process once the oxide over the anti-reflective coating is removed. A second, different etching process, is then used that selectively removes the anti-reflective coating over the gate region while preserving the oxide spacers adjacent the gate region; the spacers and gate region therein forming an aperture for receiving a silicide.

Another example embodiment of the present invention is directed to a method for manufacturing a semiconductor structure, having a substrate and a gate region thereon, that includes removing an anti-reflective coating (ARC) layer over the gate region to improve silicidation of the gate. The method includes providing a silicon oxynitride coating over an amorphous silicon gate region and providing a silicon dioxide layer over the silicon oxynitride coating layer, the gate region and the substrate. Oxide spacers are then formed on the substrate, adjacent the gate region and the silicon oxynitride coating layer, by using a first process to substantially simultaneously etch the silicon dioxide layer and to remove the silicon dioxide that is disposed on the silicon oxynitride coating. An endpoint is utilized to terminate the first process once the silicon dioxide is removed and a second, different etching process, is utilized thereafter that selectively removes the silicon oxynitride coating over the gate region while preserving the silicon dioxide spacers adjacent the gate region.

The above summary of the present invention is not intended to describe each possible embodiment or every implementation of the present invention. The figures, and the detailed description that follows, more particularly exemplify these embodiments.

Brief Description of the Drawings

The invention may be more completely understood upon consideration of the following detailed description of various embodiments of the invention in connection with the accompanying drawings, in which:

FIGS. 1A illustrates the first step of an example embodiment for making a semiconductor structure wherein the oxide layer is etched to form oxide spacers.

FIGS. 1B illustrates the example embodiment semiconductor structure after the first etching step according to the teachings of the present invention.

FIGS. 1C illustrates another step of an example embodiment for making a semiconductor structure wherein the ARC is etched from the gate region.

FIGS. 1D illustrates the example embodiment for making a semiconductor structure after another etching step according to the teachings of the present invention.

While the invention is amenable to various modifications and alternative forms, specifics thereof have been shown by way of example in the drawings and will be described in detail. It should be understood, however, that the intention is not to limit the invention to the particular embodiments described. On the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

Detailed Description

The present invention is believed to be applicable to a variety of MOS devices and semiconductor structures that utilize spacers as part of their structure or in their manufacturing process. The teachings of the present invention are believed to be applicable in the area of anti-reflective coating removal procedures prior to salicidation of a semiconductor device. A two step etching process is used to substantially remove all of an anti-reflective coating from a gate region while minimizing the dielectric spacer loss along side the gate. Minimizing spacer oxide loss along side the gate, in

turn, provides protection to the gate edge during the silicidation which prevents notching at the top of the gate. While the present invention is not necessarily so limited, an appreciation of various aspects of the invention is best gained through a discussion of various example semiconductor structures described below.

In an example embodiment, a method for manufacturing a semiconductor structure having a substrate and a gate region thereon is disclosed that involves the removal of an anti-reflective coating (ARC) layer over the gate region to improve silicidation of the gate. The method includes providing an anti-reflective coating over the gate region and providing a dielectric layer over the anti-reflective coating layer, the gate region and the substrate. Dielectric spacers are then formed on the substrate, adjacent the gate region and the anti-reflective coating layer, by etching the dielectric layer using a first process that includes selectively removing portions of the dielectric layer on the anti-reflective coating. Utilizing a second, different etching process, the anti-reflective coating over the gate region is selectively removed while preserving the spacers adjacent the gate region.

Referring now to Figures 1A-1D, Figure 1A shows a semiconductor structure having a substrate 10 with a gate region 12 disposed thereon. The gate region is made of amorphous silicon (ASi), but could be made of other compatible semiconductor materials used in the formation of gate regions. On the upper surface of gate region 12 is disposed a layer of buried anti-reflective coating (BARC) 14, which in this example embodiment is silicon oxynitride (SiON). A dielectric layer 16 is then disposed on the entire structure, which can be an oxide type material such as silicon dioxide (SiO_2). The semiconductor structure is then subjected to a first etching process step, as shown by arrows 18, wherein portions of dielectric layer 16 are primarily etched off. The first process step of a dielectric (oxide) spacer etch process will remove the BARC over the amorphous silicon and should utilize a common oxide etch chemistry such as CF4 or a mix of CHF_3/CF_4 and possibly an inert gas such as argon or helium. This step should remove all of the oxide being selective to silicon and may involve using an endpoint to terminate the etch process step once the oxide is removed. Figure 1B illustrates the

semiconductor structure after the first etching process; this figure also illustrates formation of oxide spacers 16A and 16B adjacent gate region 12 and that bound BARC layer 14.

Referring now to Figure 1C, the semiconductor structure is then subjected to the second etching process, as illustrated by arrows 20, that utilizes either a CF_4 or CHF_3 with an oxygen additive to provide selectivity to the oxide material relative to the SiON (BARC) layer 14. The etching process can be performed in either a 4520 or 4520XL using similar chamber configurations and chemistry. This method will maintain the dielectric spacer profile (16A, 16B) and minimize isolation oxide loss while ensuring complete BARC removal. Figure 1D illustrates the semiconductor structure resulting from the second etching process and illustrates that oxide spacers 16A and 16B have remained substantially intact adjacent gate region 12. Spacers 16A and 16B, along with gate region 12 now form an aperture 22 for receiving silicide during the silicidation (contact formation) process.

In this example embodiment, oxide loss is minimized in the two-step spacer etch process where the first step is a traditional oxide etch and the second step is highly selective to oxide while etching the BARC over the ASi gates. Complete BARC removal is imperative for good silicide formation on the amorphous silicon gate region. Without selectivity to the oxide material in the BARC removal process (second etch process) spacers 16A and16B widths become too small and the result is gate to source/drain leakage. In addition, notching may occur along side the amorphous silicon gate where spacer etching is excessive and has exposed this edge. Leaving oxide on the gate top edge (provided by spacers 16A and 16B – see Figure 1D) assures uniform silicide formation on top of the gate.

As noted above, the present invention is applicable to a number of different semiconductor structures and processes. Accordingly, the present invention should not be considered limited to the particular examples described above, but rather should be understood to cover all aspects of the invention as fairly set out in the attached claims. Various modifications, equivalent structures, as well as numerous structures to which

the present invention may be applicable will be readily apparent to those of skill in the art upon review of the present specification. The claims are intended to cover such modifications and devices.

What is claimed is:

1. A method for manufacturing a semiconductor structure having a substrate and a gate region thereon, comprising:

providing an anti-reflective coating over the gate region;

providing a dielectric layer over the anti-reflective coating layer and the substrate;

forming dielectric spacers on the substrate, adjacent the gate region and the anti-reflective coating layer, by etching the dielectric layer using a first process that includes selectively removing portions of the dielectric layer on the anti-reflective coating ; and

utilizing a second, different etching process, that selectively removes the anti-reflective coating over the gate region while preserving the spacers adjacent the gate region.

2. The method according to claim 1, wherein the gate region is made of amorphous silicon (ASi); and wherein the dielectric layer is formed from silicon dioxide (SiO_2).

3. The method according to claim 1, further providing an etch chemistry for the first process of CF_4 and an inert gas selected from at least one of argon and helium.

4. The method according to claim 1, further providing an etch chemistry for the first process of CHF_3/CF_4 and an inert gas selected from at least one of argon and helium.

5. The method according to claim 1, further providing an etch chemistry for the second process of an oxygen additive and at least one of CF_4 and CHF_3.

6. The method according to claim 1, wherein the dielectric spacers are oxide spacers on the substrate, adjacent the gate region and the anti-reflective coating layer, and the first process is used to substantially concurrently etch the dielectric layer to

form the spacers and to remove the dielectric on the anti-reflective coating layer; and further including utilizing an endpoint to terminate the first process once the oxide over the anti-reflective coating is removed.

7. The method according to claim 6, wherein the gate region is made of amorphous silicon (ASi), and the second, different etching process, that selectively removes the anti-reflective coating over the gate region while preserving the oxide spacers adjacent the gate region, the spacers and gate region forming an aperture therein for receiving a silicide.

8. The method according to claim 6, wherein the oxide layer is made of silicon dioxide (SiO_2) and the second, different etching process, that selectively removes the anti-reflective coating over the gate region while preserving the oxide spacers adjacent the gate region, the spacers and gate region forming an aperture therein for receiving a silicide.

9. The method according to claim 6, wherein the anti-reflective coating is made of silicon oxynitride (SiON) and the second, different etching process, that selectively removes the anti-reflective coating over the gate region while preserving the oxide spacers adjacent the gate region, the spacers and gate region forming an aperture therein for receiving a silicide.

10. The method according to claim 6, further providing an etch chemistry for the first process selected from one of CF_4 and CHF_3/CF_4, and further including an inert gas selected from one of argon and helium.

11. The method according to claim 10, further providing an etch chemistry for the second process selected from one of CHF_3 and CF_4, and further including an oxygen additive.

FIG. 1A

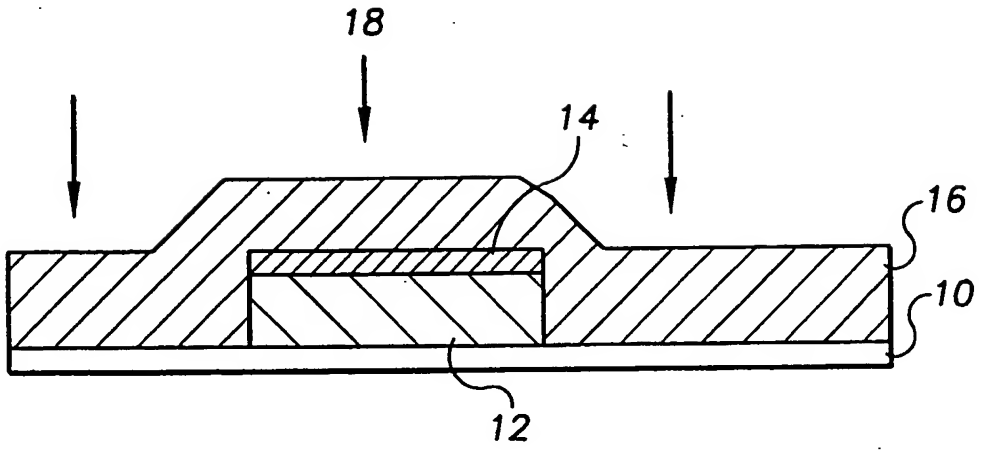


FIG. 1B

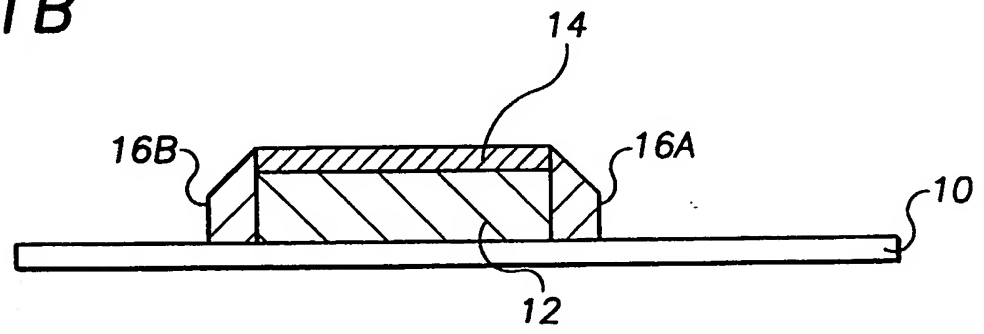


FIG. 1C

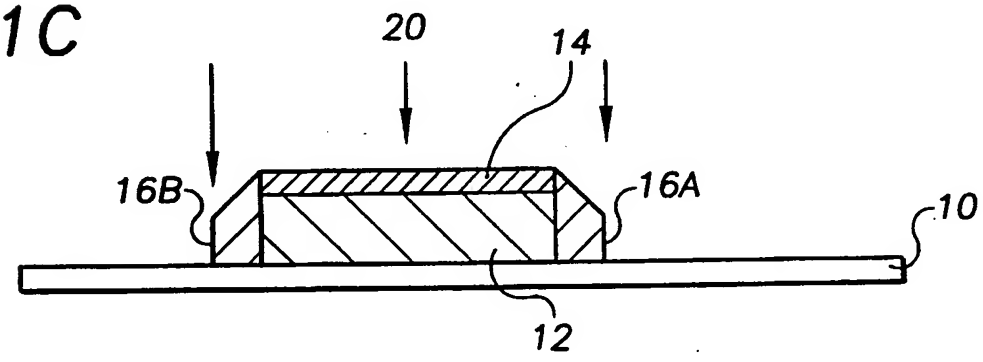
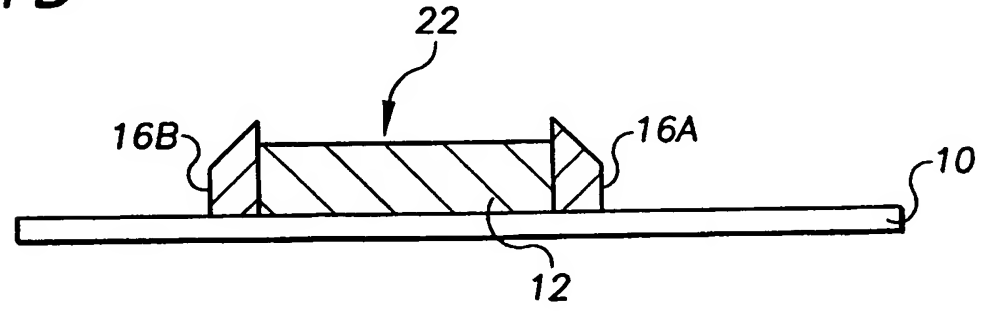


FIG. 1D



(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
12 July 2001 (12.07.2001)

PCT

(10) International Publication Number
WO 01/50504 A3

(51) International Patent Classification[7]: H01L 21/28

(21) International Application Number: PCT/US00/35130

(22) International Filing Date:
22 December 2000 (22.12.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/475,333 30 December 1999 (30.12.1999) US

(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(71) Applicant *(for MC only)*: PHILIPS SEMICONDUCTORS, INC. [US/US]; 1000 West Maude Avenue, Sunnyvale, CA 94085 (US).

(72) Inventors: HALEY, Mark, W.; 2750 CR 2615, Rio Medina, TX 78066 (US). PARKS, Delbert; 7911 Beechnut Park, San Antonio, TX 78240 (US).

(74) Agent: CRAWFORD, Robert, J.; Crawford PLLC, Suite 390, 1270 Northland Drive, Saint Paul, MN 55120 (US).

(81) Designated States *(national)*: CN, JP, KR.

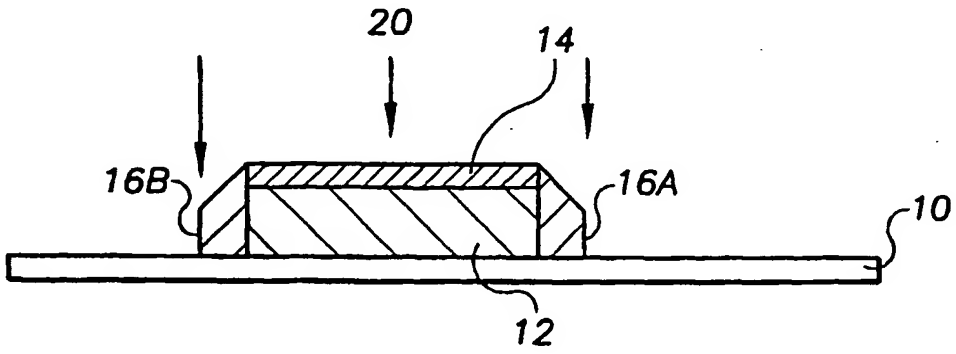
(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *with international search report*

(88) Date of publication of the international search report:
3 January 2002

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: AN IMPROVED METHOD FOR BURIED ANTI-REFLECTIVE COATING REMOVAL



(57) Abstract: A method for manufacturing a semiconductor structure, having a substrate and a gate region thereon, is described that includes removing an anti-reflective coating (ARC) layer over the gate region to improve salicidation of the gate. An anti-reflective coating is formed over the gate region and then a dielectric layer is formed over the anti-reflective coating layer and the substrate. Dielectric spacers are then formed on the substrate, adjacent the gate region and the anti-reflective coating layer, by etching the dielectric layer using a first process that includes selectively removing portions of the dielectric layer on the anti-reflective coating. Utilizing a second, different etching process, the anti-reflective coating over the gate region is selectively removed while preserving the spacers adjacent the gate region. Use of the present invention helps to minimize the dielectric spacer loss along side the gate region during removal of the buried anti-reflective coating, thereby providing a protection to the gate edge during the salicidation.

WO 01/50504 A3

INTERNATIONAL SEARCH REPORT

Int. ional Application No
PCT/US 00/35130

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/28

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 97 48127 A (GAILLARD FREDERIC ;SCHIAVONE PATRICK (FR); FRANCE TELECOM (FR)) 18 December 1997 (1997-12-18) the whole document	1-11
Y	US 5 731 239 A (PEY KIN LEONG ET AL) 24 March 1998 (1998-03-24) column 4, line 53 -column 6, line 55	1-11
Y	US 5 902 125 A (WU SHYE-LIN) 11 May 1999 (1999-05-11) column 3, line 50 -column 5, line 14	2,7
Y	US 5 880 006 A (LEE HENRY ET AL) 9 March 1999 (1999-03-09) column 3, line 60 -column 4, line 45	3-5,10, 11

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 October 2001	15/10/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Gélébart, J

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Int. ional Application No
PCT/US 00/35130

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
P,X	US 6 013 569 A (LUR WATER ET AL) 11 January 2000 (2000-01-11) column 7, line 5 - line 24; figures 5-9	1
E	US 6 194 297 B1 (CHENG CHIH-HUNG) 27 February 2001 (2001-02-27) column 2, line 42 - line 58; figure 1	1
P,X	-& DATABASE EPODOC 'Online! EUROPEAN PATENT OFFICE, THE HAGUE, NL; TW403946 B (UNITED MICROLECTRONICS CORP.), 1 September 2000 (2000-09-01) XP002179134 abstract	1
P,X	US 6 069 044 A (WU SHYE-LIN) 30 May 2000 (2000-05-30) column 1, line 50; figures 12-15 column 3, line 50 - line 54	1
E	US 6 211 048 B1 (HUNG TSUNG-YUAN ET AL) 3 April 2001 (2001-04-03) claim 9; figure 2	1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int· ional Application No
PCT/US 00/35130

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9748127 A	18-12-1997	FR 2749973 A1	19-12-1997
		EP 0904599 A1	31-03-1999
		WO 9748127 A1	18-12-1997
		JP 2000512079 T	12-09-2000
		US 6171973 B1	09-01-2001
US 5731239 A	24-03-1998	SG 64468 A1	27-04-1999
US 5902125 A	11-05-1999	NONE	
US 5880006 A	09-03-1999	NONE	
US 6013569 A	11-01-2000	NONE	
US 6194297 B1	27-02-2001	TW 403946 B	01-09-2000
US 6069044 A	30-05-2000	US 6046090 A	04-04-2000
		US 6284612 B1	04-09-2001
US 6211048 B1	03-04-2001	NONE	